REMARKS

Applicants appreciate the detailed nature of the Examiner's referenced office action, and the support for the advanced positions. Applicants also inform the Examiner of their IDS submission filed concurrently herewith. Translations of the two Japanese Kokai patent publications are not available.

Applicants have amended the specification (¶ 0079) to correct a translation artifact and to bring this paragraph into conformance with ¶ 0097, last two lines. Because support for this amendment can be found in the specification as filed, applicants submit that no new matter has been added by way of the amendment.

Applicants also submit herewith new claims directed to method embodiments of the invention. Applicants submit that these claims define over the prior art of record as well as the art being submitted concurrently herewith as part of applicants' duty of disclosure. Support in the specification for these claims can be found in the following table:

CLAIM NO.	SUPPORT IN SPECIFICATION (PARAGRAPH NO.)
27	[0066], [0067] and [0079]
28	[0086], [0067] and [0079]
29	[0066], [0067], [0079] and [0095]-[0097]
30	[0096]
31	[0095]
32	[0079]
33	[0063], [0066], [0067] and [0070])
34	[0072]

It is applicant's position that the newly presented claims define over the prior art of record. A thin film transistor (TFT) is a device in which a gate insulation film is formed on a channel region of the transistor, a gate electrode is formed on the gate

insulation film, and source/drain regions are respectively formed on both sides of the channel region. The thickness of the gate insulation film is small (on the order of nm). Because during operation of the TFT there is a high voltage potential across the gate insulation film (high voltage is applied between the gate electrode and the drain region provided on the front and back sides of the thin gate insulation film), it is very important that the gate insulation film be as free of defects as possible. A gate insulation film having fine defections and/or poor quality is considered defective for failing to maintain the trans-gate voltage potential, that is avoiding voltage breakdown.

As a method of acquiring a high quality film having no fine defection, the inventors of the subject invention, having found out that plasma density is the most important, adopt a mixture of gases of krypton and oxygen gasses, which permits excellent plasma electron density to determine plasma density. In addition, since it is important to eliminate light damage due to plasma in manufacturing the oxide film in a plasma oxidation method, it is desirable to use oxygen and xenon as a gas. By using this gas, light energy from plasma becomes 8.8eV or less, resulting in no damage to the oxide film.

Applicants submit that there is no disclosure relating to the above technical matter in references of record. Sakai simply discloses forming a silicon oxide (SiO_x) film on an electron supplying layer composed of a semiconductor with no mention of a krypton-oxygen environment. Moreover, applicants submit that this simply formed thin film cannot establish a high quality film with few occurrences of defective portions and a high dielectric value. Similarly, Ando discloses forming a silicon oxide (SiO_x) film as a gate insulation film. It, however, fails to disclose that high density plasma can be generated at a low temperature process, and that a high quality film with no occurrence of defective portions and with a high dielectric value is acquired. Takayama discloses forming a silicon nitride film and a silicon oxynitride film on a glass substrate by plasma CVD method and sputtering method. As with the other references of record, however, it fails to disclose that high density plasma can be generated at a low temperature

process, and that a high quality film with no occurrence of defective portions and a high dielectric value is acquired.

The newly supplied references are submitted as also failing to disclose or suggest the now claimed invention. The IEEE reference discloses forming a silicon oxide film at a low temperature in high density krypton plasma, but it fails to disclose acquiring a high quality film with no occurrence of defection and a high dielectric value. In addition, there is no disclosure of forming another silicon oxide on the silicon oxide film by plasma CVD. Japanese Application Patent Disclosure No. 2001-102581 discloses the use of a reaction chamber gas including Kr and O_2, maintaining substrate temperatures of 200-500°C, and using microwave energy to generate a high density plasma for forming a silicon oxide film. The reference, however, fails to disclose acquiring a high quality film with no occurrence of defective portions and high dielectric value. Importantly, however, there is no disclosure of forming another silicon oxide on the silicon oxide film by plasma CVD. Lastly, Japanese Application Patent Disclosure No.2002-208592 discloses lightly oxidizing a surface of mono-crystal silicon wafer in an oxygen gas atmosphere to form an oxidized film, and thereafter, a SiO_2 film is formed by plasma CVD method. In this reference, there is no technical disclosure on acquiring a high quality film with no occurrence of defective portions and a high dielectric value, and/or generating high density plasma in a low temperature process.

So that this response may be considered timely, applicants submit herewith a Petition for Extension of Time Under 37 CFR 1.136(a) for two (2) months. Applicants believe that no additional fees are due in connection with this response. However, should any additional fees be required, please charge them to Deposit Account No. 07-1897.

If the Examiner believes that a telephone interview would be helpful, he is respectfully requested to contact the Applicants' attorney at (425) 455-5575.

DATED this 18th day of May, 2007.

Respectfully submitted,

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